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38		1	2	3								
37		1	2	2								
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35		1	1	1								
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16		1	1	1								
15		1	1	1								
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13		1	1	1	51		1	1	1			
12		1	1	1	50		1	1	1			
11		1	1	1	49		1	1	1			
10		1	1	1	48		1	1	1			
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8		1	1	1	46		1	1	1			
7		1	1	1	45		1	1	1			
6		1	1	1	44		1	1	1			
5		1	1	1	43		1	1	1			
4		1	1	1	42		1	1	1			
3		1	1	1	41		1	1	1			
2		1	1	1	40		1	1	1			
1		1	2	3	39		1	1	1			

	Priimek in ime	Podpis	Gradivo			Odstopi netol. mer	Toplotna obdelava	Površ. zaščita	Pripadnost
									TRIGLAV
Konstr.	Urbančnik	(signature)	Izdaja	1	2	3			
Projekt.	Hafner	(signature)	Znak						
Pregled.	Rogač	(signature)	Št. obv.	11-002	11-022	11-033			
Števil.	J. Bojanić	(signature)	Datum	10.2.86	10.2.87	7.5.87			
Stand.			Podpis	(signature)	(signature)	(signature)			

Iskra Delta
proizvodnja računalniških sistemov in inženiring, p.o.

Naziv	List	Stran	J	K	Identifikacijska številka
TECHNICAL MANUAL	1				3280404 4

Namembnost kopije	Arhiv	Merilo	Sekcija	Namesto identifikacijske številke
				18842044

VME MODULE
CPU 68Ø1Ø

TECHNICAL MANUAL

Ident: 32.8Ø4.Ø44

Preliminary Version: June 1986

TECHNICAL MANUAL

Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-002					2				32804044
						Arhiv				Namesto identifikacijske številke
										18842044

Iskra Delta
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CHAPTER 1

1. GENERAL DESCRIPTION

1.1 GENERAL INFORMATION

The CPU 68Ø1Ø high performance single board computer combines the powerful 16/32 bit microprocessor, the 68Ø1Ø, with 256k/1M bytes of dynamic RAM, a maximum of 128k bytes of ROM/EPROM, and powerful I/O devices.

A wide variety of functions for the CPU 68Ø1Ø module are offered by the on-board real-time-clock, two serial I/O interfaces, the parallel port, the floating-point unit, and the timers.

The MC68451 memory management unit offers a wide variety of combinations for the transfer of logical addresses to different users, for the write protection, etc.

The interface standard corresponds to the VME bus interface. The CPU 68Ø1Ø module can be generally used in systems which are based on the VME bus.

The CPU 68Ø1Ø module has been developed as a sophisticated VME bus board which may be used in a multiprocessing enviroment as a number crunching unit, as a peripheral controller board, or as a "single-board computer" because of its I/O and timer functions.

The usage of this board in critical real-time applications is made possible by the fast on-board dynamic RAM, the increasable microprocessor clock frequency (up to 12,5 MHz), and faster address transfer from the microprocessor without using the memory management unit.

The CPU 68Ø1Ø board is technologically based on multilayer printed circuit techniques with separate internal layers for power and grounding which enable minimal signal disturbances and noise.

See the VME MODULE CPU 68Ø1Ø HARDWARE USER'S MANUAL (Ident: 29.572.Ø44) for additional information about the board, ICs, timing diagrams, timings, location diagrams, circuit schematics, data sheets, etc. The Technical Manual is just an extension of the Hardware User's Manual.

See the VME MODULE CPU 68Ø1Ø PACKAGE OF TESTING PROGRAMS (Ident: 29.638.Ø44) for additional information about testing and troubleshooting of the CPU 68Ø1Ø board.

1.2 SHORT DESCRIPTION

The basic version of the CPU 68Ø1Ø board contains the powerful 68Ø1Ø CPU, 68451 MMU (Memory Management Unit), NS32Ø81 FPU (Floating Point Unit), 1M byte of dynamic RAM, a maximum of 128K bytes of ROM/EPROM, MC146818 RTC (Real Time Clock), and several powerful I/O capabilities (see Fig.1).

The CPU 68Ø1Ø board can transfer signals/data in two basic modes to/from the VME bus, as MASTER or SLAVE. In the MASTER mode the 68Ø1Ø processor with 1Ø MHz frequency controls the transfer of data/signals to/from the VME bus. In the SLAVE mode the CPU board is one of the functional modules on the VME bus, and the transfer of data/signals can be controlled by several MASTERs. Address areas of the CPU module can be accessed by the 68Ø1Ø processor or by the MASTERs on the VME bus.

The memory management unit (MC68451 - MMU) provides the CPU board with memory management and write protection capabilities which can be different when working in user/supervisor modes, and separate for program/data transfers.

A pair of standard 28-pin JEDEC sockets enables the use of standard EPROMs or ROMs with a maximum memory capacity of 64K bytes. Therefore the maximum ROM/EPROM capacity is 128K bytes. Memory capacity of the dynamic RAM is 256K bytes or 1M byte depending on the used DRAM ICs 64K*1 or 256K*1. The DRAM transfers are controlled by the byte wide parity logic.

The I/O capabilities include serial and parallel ports. Two serial ports are supported by the RS 232 (C) standard interface with the possibility of asynchronous or synchronous data transfers, driven by the IC Z853Ø SCC. The parallel port supports the CENTRONICS standard interface for printer connection and is controlled by the Z8536 CIO, which contains also 3 Counters/Timers.

The fast floating point unit (NS32Ø81 FPU) provides excellent number crunching capabilities and supports IEEE standards for binary floating point arithmetic, Task P754.
The real time clock (MC146818 RTC) provides time, calendar functions, generation of alarms, periodical interrupts and 5Ø bytes of general purpose CMOS RAM with the possibility of battery back-up.

The one level arbitration logic and 7 level interrupt logic operate according to the VME bus principles.

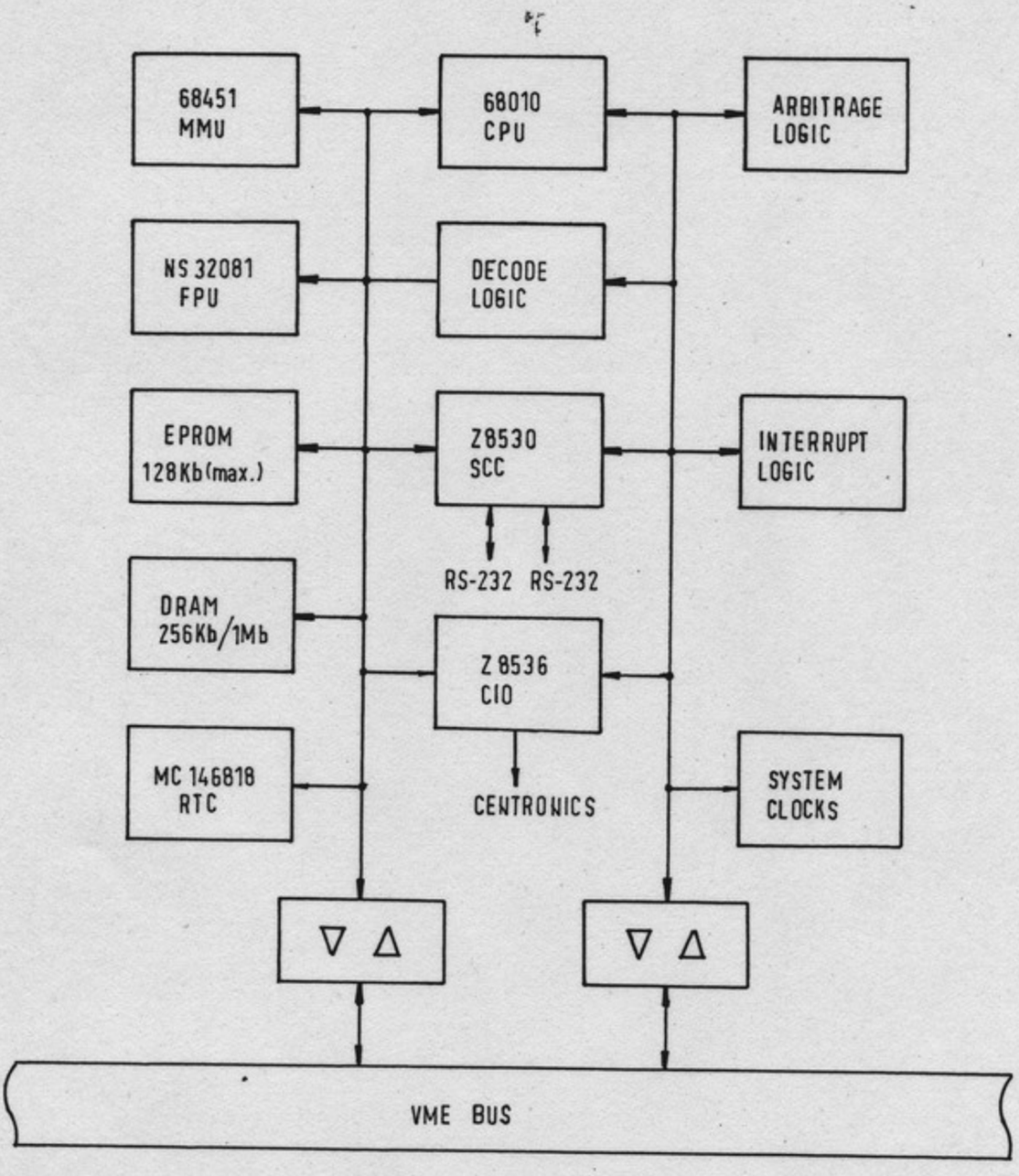

Figure 1: CPU MODULE 68010 SCHEMATIC DIAGRAM

Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-002					8				32804044
Iskra Delta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv				Namesto identifikacijske številke: 18842044

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1.3 TECHNICAL SPECIFICATIONS

Bus Interface	Standard VME bus interface
Microprocessor	MC68Ø1Ø (1Ø MHz)
Memory Management Unit	MC68451 (1Ø MHz)
Floating-Point Unit	NS32Ø81-6 with single precision (32-bit), double precision (64-bit) binary floating-point arithmetic, according to the IEEE specifications, Task P754
Parallel I/O	CENTRONICS parallel interface (Z8536 CIO)
Serial I/O	2 RS 232 (C) interfaces, programmable baud rate from 5Ø to 192ØØ bauds (Z853Ø SCC)
Timers	3 16-bit timers (Z8536-CIO)
Real Time Clock	MC146818 with 5Ø bytes of CMOS RAM with the possibility of a battery back-up
Memory	1 Mbyte of DRAM with byte parity, 64K bytes of EPROM (max. 128K bytes)
Power Requirements	+5V +-5%, typically 3,ØA, maximum 3,3A, +12V +-5%, typically 4ØmA, maximum 5ØmA, -12V +-5%, typically 2ØmA, maximum 3ØmA.
Operating Temp.	Ø to 7Ø degrees C
Storage Temp.	-5Ø to 85 degrees C
Relative Humidity	Ø-95% (non-condensing)
Board Dimensions	Double Eurocard 234x16Ømm (9.2x6.3")
Configuration	DTB Master: A24, D16 or DØ8, DTB Slave: A24, D16 or DØ8, DTB Requestor: any from 1-4, one or more CPU modules on the VME bus.
Options	- 256K bytes of DRAM with byte parity, - MC68Ø1Ø (12.5,1Ø,8,6 or 4 MHz) with or without MC68451 MMU, - MC68ØØØ (12.5,1Ø,8,6 or 4MHz) without MC68451 MMU.
Ordering No.	188 42Ø Ø44 CPU 68Ø1Ø.

CHAPTER 2

2. FUNCTIONAL DESCRIPTION

2.1 MICROPROCESSOR

Two different microprocessors can be used on CPU 68Ø1Ø/68ØØØ boards, the 68Ø1Ø or the 68ØØØ, with 1Ø MHz clock frequency, which can be changed to 4, 6, 8 or 12.5 MHz according to the user needs. When the 68ØØØ processor is to be used, the MC68451 MMU should be replaced with a wired "piggy-back".

2.2 MC68451 MEMORY MANAGEMENT UNIT (MMU)

The MC68451 Memory Management Unit (MMU) provides address translation and protection for the 16M byte addressing range of the 68Ø1Ø microprocessor, which provides function code signals and addresses during each bus cycle. The function code specifies an address space and the address specifies a location within that address space.

The 68451 MMU is the basic element of a memory management mechanism on the CPU 68Ø1Ø board. Address translation is provided only when the 68Ø1Ø processor is MASTER. The MMU provides the 68Ø1Ø with the capability to allocate, control, and protect system memory. The MMU can be programmed to cause an interrupt when a selected section of memory is accessed, and it can directly translate a logical address into a physical address making it available to the 68Ø1Ø processor. Using these features, the MMU can provide separation and security for user programs and allow the operating system to manage the memory in an efficient fashion for multitasking.

After activation of the RESET- signal, the MMU acts as if it was not present on the CPU 68Ø1Ø board. So, logical addresses from the 68Ø1Ø processor are equal to physical addresses from the MMU.
The MMU works in S2 mode because the pin MODE of the MMU is connected to the ground. The FC3 signal on the MMU (pin B8) is generated by the BGACK+ signal, which is the negated BBSY* signal from the VME bus. The MMU generates the necessary signals for demultiplexing of data signals DØØ-D16 (signal ED-) in the ICs 74LS373 on positions E19 and E17 and address signals AØ8-A23 (signal HAD-) in the ICs 74LS245 on positions E18 and E2Ø.

The PAL 16L8 on position E36 is used for the generation of the PAS-, PLDS-, PUDS-, RW- , DIR-, EN- and DS signals:

- the PAS- (Physical Address Strobe) signal is active when the MAS- signal from the MMU and the AS- signal from the 68Ø1Ø processor are active. It can be activated only when the 68Ø1Ø is MASTER.

- the PLDS- and PUDS- (Physical Upper, Lower Data Strobe) signals are active, when the AS- and MAS- signals and data strobes from the processor are active (UDS-, LDS- signals), and the read cycle is to be performed. At write cycle PLDS- and PUDS- signals are activated only if the WINI- (Write Inhibit) signal from the MMU is not active. So, data can not be written to the segment, which is write protected.

- the R/W- signal is a duplicated R/WI- signal from the 68Ø1Ø processor for the reason of the great fan-out.

- the DIR- signal controls the direction of data signals in ICs 74LS645-1 on positions E1 and E6. It is controlled by the signals R/WI and BGACK-. Data are transferred to the VME bus when the CPU 68Ø1Ø board is MASTER and write cycle is to be performed or when another MASTER on the VME bus performs the read cycle. Data are read from the VME bus when the 68Ø1Ø processor performs the read cycle from the VME bus or when another MASTER on the VME bus performs the write cycle to the CPU 68Ø1Ø board.

- the EN- signal enables data transfers to/from the VME bus. It can be activated when the 68Ø1Ø processor is MASTER and its address is from the CPU 68Ø1Ø address area or interrupt acknowledge cycle on the VME bus in progress. When there is another MASTER active on the VME bus, the data transfer to/from the CPU 68Ø1Ø board is performed only if the CPU board is selected.

- the DS+ signal is activated if at least one of the PLDS-, PUDS- signals is activated.

2.3 DYNAMIC RAM

The DRAM area consists of 1M byte of Dynamic RAM on the basic version of the CPU 68Ø1Ø board, with the 256K*1 ICs used, and with byte parity.

The DRAM area is reduced to 256K bytes with the 64K*1 ICs used, and with byte parity.

The NS84Ø9 DRAM Controller is used for refreshing and DRAM controlling.

DRAM ICs on positions ML0-ML15 are used for writing/reading lower data bits (DØØ-DØ7), and DRAM ICs on positions MUØ-MU15 are used for writing/reading upper data bits (DØ8-D15).

2.3.1 DRAM PARITY LOGIC

The CPU module uses parity logic for checking the parity of written/read data. For each data byte its own parity bit is generated. In the IC 74S28Ø on position E29 the parity bit for lower data bytes (DØØ-DØ7) is generated/checked, which is read/written in the memory elements on positions PL0 or PL1. In the IC 74S28Ø on position E3Ø the parity bit for upper data bytes (DØ8-D15) is generated/checked, which is read/written in the memory elements on positions PUØ or PU1. Memory elements for storing parity bits must have equal memory capacity as memory elements of the DRAM memory.

Parity checking is executed at each reading from the DRAM memory in the IC PAL 16R4 on position E38. When the CSDRAM-, DTACK-, RW, PUDS-, or PLDS- signals are active, and one of the parity signals is active (pins 8,9 on the PAL 16R4 on position E38), the MBERR- signal activates the BERR- signal to the 68Ø1Ø processor. The MBERR- signal can be activated also by the BERR* signal on the VME bus by the BERRI- signal if the DRAM is not selected and bus cycle is in progress. In the SLAVE mode, when reading data from the DRAM to the VME bus, parity error can be signalled over the IC 74LS32 on position E4Ø to the VME bus. The DTACKO signal (the delayed DTACK- signal of the DRAM when the CPU 68Ø1Ø works in the SLAVE mode) can be asserted only if there is no parity error during the read cycle from the DRAM. The DTACKO signal activates the DTZ signal over the IC 74LS32 on position E4Ø and the DTZ signal activates the DTACK* signal on the VME bus over the 74LS641-1 on position E15.

After system power-up, data and parity bits are optionally set and should be written before they are read. Therefore it is necessary to overwrite the DRAM memory after the power-up of the system to set the parity and data bits. The PERCLK signal must be active before using the DRAM.

Regarding the DRAM memory elements, it is possible to adjust the assertion of the data transfer acknowledge signal (DTACK-) with the BR11 jumper, which should be inserted only for devices with an access time of 120 ns or better.

The assertion of the DTACK- signal is based on the 20 MHz clock (CLKX signal) in the PAL 16R6 on position E4. Signals C2, C1, C0 are derived from the previously mentioned 20 MHz clock and count clocks after the assertion of the DS+ signal. So, the assertion of the DTACK- signal is based on the counters, which count in 100 ns wait cycle increments. The number of wait cycles is the following:

	type of transfer	
setting of the BR11 jumper	MASTER CPU 68010 or select from the VME bus (write cycle)	select from the VME bus (read cycle)
	number of wait cycles	
inserted /120 ns ICs/	0	1
removed /150 ns ICs/	1	2

It is also possible to adjust the assertion speed of the DTACK- signal with the change of functions in the PAL 16R6 on position E4.

The DRAM can be addressed on byte and word basis. Read-modify cycles are also provided. The DRAM has an access time of 120 ns (maximum) if no refresh cycle is under execution.

For VME bus compatibility, DRAM access times are delayed for 100 ns when the DRAM is selected from the VME bus, and read from the DRAM is performed. So, parity checking can be performed on time. When the BERR* signal from the parity logic on the VME bus is asserted, the DTACK* signal on the VME bus is not asserted.

2.3.2 DYNAMIC RAM REFRESH LOGIC

The Dynamic RAM refresh is accomplished by performing a memory cycle at each of the 128 row addresses at an interval of less than 2 ms. The used "RAS Only Refresh" results in a substantial reduction of operating power. The refresh is fully asynchronous to the local and VME bus accesses.

The DRAM memory is controlled by the IC DP8409 - DRAM Controller on position E5. The DRAM Controller works in MODE5 with hidden refreshes.

The Refresh requests are generated by the DRAM Controller according to the PERCLK signal with the 15,2 microsecond period. For selecting data banks the RAS1- and RASØ- signals are used, depending on the state of the A1 signal. The DRAM refreshing depends on the RESET- and HALT- state of the 68Ø1Ø processor, addressing the outside address range and other MASTER's on the VME bus, so the refresh logic is controlled by the IC PAL 16R6 on position E4 with regard to the mentioned states.

The DRAM Controller performs a hidden refresh in the first half of the PERCLK signal if it is possible. The hidden refresh is possible if the bus cycle is in progress and the DRAM is not selected and is performed automatically. If the refresh is not performed in the first half of the PERCLK signal, the DRAM Controller sends a request for a forced refresh to the PAL 16R6 on position E4 by activating the RFIO- signal on pin 46. The PAL logic performs a hidden refresh in the active part of the system cycle (PAS- active) by the activation of the M2-RFSH signal to the DRAM Controller, pin 5, if the DRAM is not selected in that cycle. If the DRAM is selected, a forced refresh is performed at the end of the current DRAM access cycle, and the next (possible) DRAM access is delayed for a maximum of 8ØØ ns. In this situation the RASIN- signal (Row Address Select signal) to the DRAM controller is blocked by the RASI signal from the PAL 16R6 on position E4 and the M2-RFSH signal is activated to the DRAM Controller.

2.4 ROM/EPROM

The CPU 68Ø1Ø ROM/EPROM area consists of 2 28-pin sockets for JEDEC Compatible devices.

The Socket on position E25 is used for reading the lower 8 data bits (DØØ-DØ7), the socket on position E16 is used for reading the upper 8 data bits (DØ8-D15). Writing to the ROM/EPROM address area is not possible and is not acknowledged with the data transfer acknowledge signal (DTACK-). The write cycle is completed with the Bus Time Out error (BTO-).

The ROM/EPROM address area occupies with elements 27256 64k bytes of the CPU module's address area. With the address area decrease or increase in the decode logic, and with the adjustment of the BR6, BR8 and BR13 jumpers, EPROMs with different capacity can be used.

The ROM/EPROM area can be configured for the following devices:

Device	Type	Capacity	Total ROM/EPROM Capacity
EPROM	2764	8k*8	16k bytes total
EPROM	27128	16k*8	32k bytes total
EPROM	27256	32k*8	64k bytes total
EPROM	27512	64k*8	128k bytes total

The connection of address signals for the different device types is provided by the BR13, BR8 and BR6 jumpers.

The decode logic of ROM/EPROM address area is provided for 27256 devices. When EPROMs with smaller memory capacity are used, only part of the decoded ROM/EPROM address area is used effectively, in the rest of the ROM/EPROM address area the contents of the used ROM/EPROM is multiplied.

The following table shows all the jumper settings which are required for the different EPROMs:

EPROM	BR13 setting	BR8 setting	BR6 setting
2764	3-4	3-4	3-4
27128	3-4	1-2	3-4
27256	3-4	1-2	1-2
27512	1-2	1-2	1-2

The default setting of the decode logic and jumpers BR13, BR8 and BR6 during manufacturing is provided for the 27256 devices with 250 ns access time or better.

With regard to the used EPROM elements it is possible to adjust the assertion of the data transfer acknowledge signal (DTACK-) with the change of the function in the PAL 16R6 on position E4. The assertion is delayed for 2 wait cycles (200 ns) and is provided for 250 ns devices.

Reading from EPROMs is possible on byte and word basis. Part of the ROM/EPROM address area ($FE0008 - $FE03FF) is used for address areas of the CIO, SCC, FPU, MMU and RTC.

2.5 REAL TIME CLOCK (RTC)

The on-board Real Time Clock (RTC) - MC146818 can be used as a calendar, a real time counter and for time measurements.

The Real Time Clock is located on position E32. It is driven by a crystal which generates a periodical signal with 4,19 MHz frequency on position Q1. Frequency setup can be adjusted by the variable capacitor CK6 and should be equal to 4.194304 MHz. Multiplexing of data and address signals when the addressing of the RTC is performed is provided by IC 74LS245 on position E27 for the data, and by IC 74LS244 on position E26 for the address signals. It is controlled by the ARTC and DRTC signals from PAL 16R4 on position E38. The ARTC signal is activated when the RTC is selected and the E signal from the 68010 processor 68010 is in the low state and provides the transfer of address signals to the RTC. The DRTC signal is activated when the RTC is selected and the E signal from the 68010 processor is in the high state and provides the transfer of data signals to/from the RTC. The DRTC and ARTC signals are active in the low state.

The select signal for the RTC is connected to the signals for battery back-up from the VME bus (+5V STBY line) and provides the RTC operation at power-down with minimal power consumption. Beside standard time and calendar functions, alarm and periodical interrupts, RTC contains also 50 bytes of CMOS RAM which saves data when power is off.

Addressing is possible on byte basis, i.e. on odd addresses. When addressing is carried out on word basis, only the lower data byte is transferred (D00-D07).

The RTC is a device from the 6800 synchronuos family. Therefore, the access cycle is controlled by the processor signals VMA-, VPA- and the E signal.

To initiate the transfer, the processor must receive the VPA- signal from the decode logic. When the CPU is synchronized with the E clock signal, the VMA- signal is asserted to signal the I/O devices that the transfer is beginning. The synchronization requires additional time (1000 ns maximum).

2.5.1 RTC INTERRUPT SCHEME

The RTC can be used to force an interrupt to the on-board CPU. The RTC interrupt request level is fixed at level 6, the highest maskable interrupt level.

The interrupt control logic is handled by the IC PAL 16L8 on position E44. The interrupt control logic on the board decodes the RTC interrupt request level (IRQ6-) and forces the auto-interrupt vector, after the interrupt has been acknowledged on that level. This vector is fixed and reserved on the board specially for the RTC. The long word stored at the $00000078 address (vector no. 30) represents the RTC interrupt handling routine jump address.

2.6 Z8536 CIO

The IC Z8536 CIO contains 3 ports and 3 counters/timers which can all be software programmed. The CIO includes also the interrupt logic, the pattern-recognition logic, 1's catchers, programmable open drain outputs, etc.

The Generation of the RD-, WR-, CLR and DTACK- signals when adressing the CIO, is handled by IC PAL 16R6 on position E36, which is controlled by the 20 MHz CLKX signal. The CLK and the PCLK clocks are 10 and 5 MHz clocks, derived from the CLKX clock divided by 2 and 4. C3, C2 and C1 signals are clocks for the activation of RD-, WR- and DTACK- signals. Clock C1 is activated only if the address signal IA5 is in the low position and separates the address area of the CIO of the address area of the FPU. The WR- signal can be activated when the write cycle to the CIO (SCC) is performed and when the RES0- signal is activated (initial power-up reset of the CPU 68010 board). The RD- signal can be activated when the read or interrupt acknowledge cycle from the CIO (SCC) is performed and when the RES0- signal is activated. The DTACK- signal is activated when the CIO, SCC or FPU is selected and when the interrupt acknowledge cycle from the CIO or SCC is in progress.

The CIO and SCC are driven by the 5 MHz PCLK clock signal.

The CIO is used for the transfer of the control/data signals to the printer with the CENTRONICS interface. The 3 timers are provided for the generation of the periodical interrupt to the 68010 CPU, the generation of the PERCLK periodical signal to the DRAM Controller NS8409, and for the generation of the BTO- (Bus Time Out) signal.

Addressing on byte basis is possibble, with addressing on word basis only the lower data byte is transferred (D00-D07).

The Z8536 CIO supports the standard CENTRONICS parallel interface. This interface allows the connection of a CENTRONICS compatible printer, whereas the handshake protocol is under the CIO's interrupt and the 68010 processor's interrupt and program logic. The output signals are driven by the 7407 devices, which have a drive capacity of 40 mA. This allows a cable length of approximately 5 metres to the printer.

Port A of the CIO is used for the transfer of data signals (DØØ-DØ7) to the printer. The handshake control signals for printer control are handled by Port B of the CIO. The connector for the signal/data transfer to/from the printer by the CENTRONICS interface is on position P5.

The PAPEREND+ and FAULT- signals report an error condition over the IC 74LSØ8 on position E42 to Port B, bit 3 of the CIO. The voltage fail (ACFAIL*) and system error (SYSFAIL*) signals also enter to Port B, bits PB6 and PB7.

The STROBE- (DATA STROBE-) signal to the printer, when transferring data to printer, must be software programmed on Port C, bit D3, pin 22, of the CIO.

2.6.1 Z8536 CIO COUNTERS/TIMERS

The CIO contains 3 software programmable 16-bit counters/timers (C/T).

The Counter/timer No. 1 is provided for the generation of the periodical interrupt to the 68Ø1Ø processor.

The counter/timer No. 2 generates the PERCLK periodical signal to the NS84Ø9 DRAM Controller from Port B, bit PBØ, pin 8 of the CIO, with a period of 15,2 microseconds.

The counter/timer No. 3 is provided for error generation when the address from the 68Ø1Ø processor is outside the address range of the configuration (Bus Time Out error). The trigger for the counter/timer No. 3 is the DS+ signal, which enters to Port C, bit 2, pin 21 of the CIO. The Counter/timer No. 3 signals the BTO- error from Port C, bit Ø, pin 19 of the CIO , by activating the BERR- signal.

The output from Port C, bit Ø, should be in the CIO programmed as an open-collector output. The time adjustment for signalling the BTO- error can be set up (programmed) to 26 ms by counter/timer 3.

The MBERR- signal is connected to the CIO, port C, bit 1, pin 2Ø.

The CIO has a higher priority than the SCC and enables the acknowledgement of the SCC interrupts by the IECIO signal. The IC FPU can not provide an interrupt vector, therefore the interrupt request from the FPU is connected to Port C, bit 5 of the CIO, which generates the interrupt request to the 68Ø1Ø processor and sends the interrupt vector. The CIO is on position E45 on the CPU module.

2.7 Z8530 SCC

The IC Z8530 SCC provides the CPU 68010 module's connection to two RS 232 (C) channel interfaces. The RD-, WR-, CLK and DTACK- signals are generated from the IC PAL 16R6 on position E39 in the same manner as for the CIO.

Different options for the transmit/receive signals, and the use of male/female connectors for the RS 232 channels are made possible by the adjustment of the J5, J5A, J6A, J6, J5B, J6B jumpers. The use of female connectors is provided for the RS232 P3 and P4 connectors but male connectors can also be used.

The channel A connector is on position P4 and the channel B connector is on position P3. Byte addressing is possible, word addressing transfers only the lower data byte (D00-D07).

The Z8530 SCC can interrupt the 68010 microprocessor on level 6.

2.7.1 SCC JUMPER ADJUSTMENT

The CPU 68010 board is designed for the use of female or male connectors for the RS 232 (C) channels. If it is necessary to replace the female connector with the male connector, pins 9, 10, 11, 13, 19, 22, 24 on the connector must be cut.

Jumper adjustments for the RS 232 ports are very variable.

Adjustment during the manufacturing is the following:

CHANNEL A SIGNAL ASSIGNMENTS:

J6-PIN	P4 PIN	INPUT	OUTPUT	SIGNAL DESCRIPTION
	1	X	X	Protective GND not connected to signal GND
7-40	2		X	Transmit Data (TXD)
5-42	3	X		Receive Data (RXD)
	7	X	X	Signal GND

CHANNEL B SIGNAL ASSIGNMENTS:

J5 PIN	P3 PIN	INPUT	OUTPUT	
	1	X	X	Protective GND not connected to the GND signal
7-40	2		X	Transmit Data (TXD)
5-42	3	X		Receive Data (RXD)
	7	X	X	Signal GND
13-34		X	X	Internal CTS (+12V)
22-25	20	X		Data set ready (DSR)

2.8 NS32081 FPU

The IC NS32081 FPU - Floating Point Unit provides a fast floating-point capability for the 68010 processor.

The FPU select is performed by the IC PAL 16R6 on position E39 to the IC 74LS10 on position E41, and IC 7407 on position E55 to pin 21 of the FPU. On the same pin the FPU signals the end of operation execution to the CIO. Therefore when the interrupt logic from the FPU is used, the CIO should be properly programmed. The FPU system clock is generated by the IC PAL 16R6 on position E39, the 5 MHz signal is signed PCLK.

FPU addressing is possible only on word basis. The IC PAL16R6 on position E39 at byte addressing does not generate the select signal for the FPU and the signal for the data transfer acknowledge (DTACK-).

The FPU is located on position E21 on the CPU module. The 6 MHz version of the IC NS32081 is used.

2.9 CPU 68Ø1Ø CLOCKS

The system clock (SYSCLK) can be generated from the CPU 68Ø1Ø module to the VME bus, or the CPU module can receive the SYSCLK signal from the VME bus. That depends on the jumper adjustment. Jumper set-up also provides clocks for driving the CIO, SCC, FPU, and DRAM Controller, the 68Ø1Ø processor, and MMU and PALs, which are clock-driven.

If the CPU module provides the SYSCLK signal to the VME bus, it is necessary to adjust:

THE CPU 68Ø1Ø CLOCK DEFINITIONS:

DESCRIPTION	BR1	BR4	BR12
SYSCLK from the VME bus	X	1-2	-
SYSCLK to the VME bus	X	3-4	1-2
2Ø MHz internal synchronization	3-4	X	X
16 MHz internal synchronization	1-2	X	X
Factory adjustment	3-4	3-4	1-2

The oscillator for generating the 16 MHz SYSCLK signal is on position Q3. The oscillator for generating the 2Ø MHz CLKX internal synchronization signal is on position Q2.

If The SYSCLK signal is received from the VME bus, the BR4 jumper should be connected to 1-2.

The CIO, SCC, FPU and DRAM Controller, the 68Ø1Ø processor, the MMU and PAL ICs work on the basis of the 2Ø MHz internal clock. The 2Ø MHz clock is divided to 1Ø MHz (CLK signal) by the IC PAL 16R6 on position E39 for driving the 68Ø1Ø processor, the MMU, and the DRAM Controller, and to 5 MHz (PCLK signal) for driving the CIO, SCC and FPU. The IC PAL 16R4 on position E14, the PAL 16R6 on position E4, the PAL 16R4 on position E38, and the PAL 16R6 on position E39 work on the basis of the 2Ø MHz clock. The signal is called CLKX and is enabled by the connection 3-4 on the BR1 jumper.

The CIO, SCC, FPU and DRAM Controller, the 68Ø1Ø processor, the MMU and PAL ICs can be also driven by the SYSCLK signal, which can be provided by the CPU module or by the VME bus. Signal SYSCLK is divided in the IC PAL 16R6 on position E39 to 8MHz for driving the 68Ø1Ø proccesor, the MMU, and the DRAM Controller, and to 4 MHz for driving the CIO, SCC, and FPU. It is necessary to set the BR1 jumper to 1-2 in that case. The PALs which are driven by the above mentioned 2Ø MHz clock, are driven in the latter case with the 16 MHz clock, labeled SYSCLK.

2.1Ø CPU 68Ø1Ø DECODE LOGIC

Address decoding of the CPU module addresses and of the input/output address area is performed by the IC PAL 14L4 on position E35 for adresses A23-A12, the FC2 signals, and the BGACK+ signal for the generation of DRAMI-, I/O-, EPRI- and PER- signals (pin 17). The address decoding is continued by the IC PAL 16L8 on position E32 for adresses A22-AØ3, for the output signals from the already mentioned PAL, and signals for the address area decoding inside the CPU module are generated.

THE CPU 68Ø1Ø ADDRESS DECODING:

INPUT SIGNALS /PAL 14L4/														OUTPUT SIGNALS
BGACK	FC2	A23	A22	A21	A2Ø	A19	A18	A17	A16	A15	A14	A13	A12	
1	X	1	1	1	1	1	1	1	1	X	X	X	X	I/O-
X	X	1	1	1	1	1	1	1	Ø	Ø	Ø	Ø	Ø	PER-
X	X	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	
X	X	1	1	1	1	1	1	1	Ø	X	X	X	X	EPRI-
X	X	Ø	Ø	Ø	Ø	X	X	X	X	X	X	X	X	DRAMI-

Note: In decode tables states of input signals are used, all output signals are active in the low state.

INPUT SIGNALS /PAL 16L8/													OUTPUT SIGNAL
DRAMI-	EPRI-	PER-	A11	A1Ø	A9	A8	A7	A6	A5	A4	A3	CSEPR-	
X	X	Ø	Ø	Ø	1	X	X	X	X	X	X	X	CSRTC-
X	X	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	X	CSSCC-
X	X	Ø	Ø	Ø	Ø	Ø	Ø	Ø	X	1	Ø	X	CSCIO-
X	X	Ø	Ø	Ø	Ø	Ø	Ø	1	X	X	X	X	CSMMU-
Ø	Ø	X	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	X	CSEPR-
1	Ø	1	X	X	X	X	X	X	X	X	X	X	
1	Ø	Ø	1	X	X	X	X	X	X	X	X	X	
1	Ø	Ø	X	1	X	X	X	X	X	X	X	X	
Ø	1	X	X	X	X	X	X	X	X	X	X	X	CSDRAM-
Ø	Ø	X	X	X	X	X	X	X	X	X	X	1	

The decoding signal for the FPU is generated in conjuction with the active signals CSCIO-, DS+ and A5 in the IC74LS1Ø on position E41. When adressing the CIO, the CSCIO- signal is active and the A5 signal is in low state on the IC 74LS32 on position E4Ø.

The CPU module generates also the AM (Address Modifier) signals when addressing the addresses outside the CPU module's address space. AM signals are driven by the 68Ø1Ø CPU board when working as MASTER:

AMØ - same as signal FC0 from the 68Ø1Ø processor
AM1 - same as signal FC1 from the 68Ø1Ø processor
AM2 - same as signal FC2 from the 68Ø1Ø processor
AM3 - always logical "1"
AM4 - same as signal I/O- from the decode logic
AM5 - always logical "1".

If the CPU module is not MASTER, it receives and decodes the addresses inside the CPU module's address area on the basis of the state of the signal AM2 (FC2).

The logic in the PAL 14L4 on position E35 can be changed to achieve different addresses areas of the DRAM, EPROM, FPU, MMU, CIO, SCC and RTC when the CPU 68Ø1Ø module works as MASTER/SLAVE, in the USER/SUPERVISOR mode, depending on the state of the signals BGACK+ and FC2 (AM2).

2.11 I/O ADDRESS AREA

The I/O address area occupies the addresses $FF0000 - $FFFFFF. When adressing these addresses, the CPU module drives AM signals according to the VME bus standards. The addressing can be on byte, word or long word basis. The decode logic of the CPU module decodes the I/O address area only when the CPU module is MASTER.

2.12 VME BUS INTERFACE

If the CPU 68010 board is the current VME bus MASTER and the current access address is higher than or equal $100000, then the VME bus transfer is initiated.

The VME bus defines the address modifier signals, which in turn define the access type that is under execution. When the CPU 68010 is MASTER, it can activate only the combinations of address modifier signals with the codes: 3E, 3D, 3A, 39, 2D and 29.

See the time values and diagrams in the VME MODULE CPU 68010 HARDWARE USER'S MANUAL.

2.13 BUS ERROR FUNCTION

A time-out counter is used on the board to provide an error function if a device or memory on the VME bus has not responded within a maximum time.

This time-out counter generates a bus error signal (BERR-) after the programmable time limit (up to 26 ms) in the C/T3 of the CIO. The CPU aborts the current cycle if the BERR- signal has been recognized and forces the exception routine.

If the board is the current VME bus MASTER and an external VME bus card generates a BERR*, then the cycle will be aborted in the same way, because the VME bus BERR* signal is ANDed with the internal time-out counter BERR- signal, and the parity control logic of the CPU 68010 board's DRAM.

2.14 CPU 68Ø1Ø INTERRUPT HANDLING

The on-board CPU is able to handle 7 different prioritized interrupt request levels, according to the VME bus principles.

To provide full VME bus compatibility, the IACK* signal is driven as an output signal if the CPU 68Ø1Ø board is the current VME bus master. This allows full multi-processing in high performance systems because of transparent interrupt handling of the on- and off-board IRQs.

The low driven IACK* signal is wired to slot one of the VME mother board and runs down the IACK daisy-chain.

The interrupt logic of the CPU module is handled by the IC PAL 16L8 on position E44. All interrrupts which come from the MMU, RTC, SCC, CIO (here is also the interrupt from the FPU), are signalled by the PAL 16L8 on position E44 with the IRQ6- signal by the IC 74LS148 to the 68Ø1Ø processor on level 6. The interrupt logic handles interrupt requests and acknowledges from the elements inside the CPU module and from the bus when the CPU module is MASTER, but the CPU module does not request interrupts if the VME bus is handled by another MASTER.

When the 68Ø1Ø processor acknowledges an interrupt, the priority of the generating interrupt acknowledge vector is the following: RTC, CIO, SCC, MMU from the highest to the lowest. In the IC PAL 16R4 on position E44 it is possible to change the interrupt priority with the change of the internal priority daisy-chain. The MMU, CIO and SCC acknowledge the interrupts by sending the interrupt vector, but RTC works on the auto-vector basis, without sending the interrupt vector. Thus, the interrupt vector from the RTC can not be changed like the other three interrupt sources, and the 68Ø1Ø processor always takes the vector address from the $ØØØØ78 address.

If the interrupt request is pending on level 6 from the VME bus, and at the same time one of the interrupt requests inside the CPU module is pending, then the last request is executed first.

The NS32Ø81 FPU interrupt requests and acknowledges are handled by the Z8536 CIO, which should be programmed proprerly when the interrupt logic from the FPU is to be used.

2.14.1 ACFAIL*, SYSFAIL* INTERRUPT HANDLING

The CPU 68Ø1Ø module receives ACFAIL*, SYSFAIL* signals from the VME bus. Interrupt requests and acknowledges for these two signals are handled by the Z8536 CIO, which receives SYSFAIL* and ACFAIL* signals on Port B, and requests interrupt on the level 6.

Signals SYSFAIL* and ACFAIL* have the highest priority of all interrupt requesting signals on Port B of the CIO.

Activation of the ACFAIL*, SYSFAIL* signals is to be performed by the VME bus, only the signal activation detection and handling of the voltage drop (ACFAIL*) and system error (SYSFAIL*) state on the VME bus are to be handled by the CPU 68Ø1Ø board.

2.15 VME BUS ARBITRATION

One level of the DTB MASTER and one level of the DTB SLAVE arbitration is provided on the board to allow the use of the CPU 68Ø1Ø in multi-master and multi-processor environments.

Arbitration logic works according to the principles of the VME bus interface. The IC PAL 16R4 on position E14 controls arbitration requests depending on the definition of the CPU module to work as ARBITER or not, which can be defined by jumper BR3. The 1-2 connection determines that the CPU module works as SLAVE and requests the bus from the current ARBITER. The removed connection causes that the CPU module works as ARBITER, which allows the control of the bus to other MASTERs on the VME bus. The CPU module receives/transmits signals for the arbitration requests handling only on one level. The level can be adjusted by the jumpers on position J1 (input/output signals BRØ* - BR3*, BGØ* - BG3* IN or OUT).

When working as MASTER, the CPU module eg. the IC PAL 16R4 on the E14 position drives the BGXOUT* signal (X=Ø,1,2 or 3) after the completed last cycle of the 68Ø1Ø processor when the AS- signal is already inactive. The PAL logic delays the signal BR- to the 68Ø1Ø processor for 5Ø ns in case that the MASTER on the bus simultaneously activates the BBSY* signal and inactivates the bus request (signal BRX, X=Ø,1,2 or 3). The CPU 68Ø1Ø board arbitration works on the ROR (Release On Request) principle. When working in the SLAVE mode, the CPU 68Ø1Ø module activates BRX* line (X=Ø,1,2 or 3) immediately after the system RESET if none of the MASTERs on the VME bus is active, or when any of the internal interrupt requests is pending. The bus arbitration then functions according to the VME bus principles. After the BGIN* signal has been received on the equivalent level, the control logic drives the BBSY* signal low to inform the Bus Arbiter that the arbitration is completed, and releases its Bus Request signal.

The Bus Request level and the Bus Grant level must be the same for a proper operation. The default Bus Request level during manufacturing is 3.

BRX, BGXIN, BGXOUT ADJUSTMENT:

JUMPER CONNECTION	SIGNAL ENABLED
1 - 24	BGØIN*
2 - 23	BGØØUT*
3 - 22	BG1IN*
4 - 21	BG1ØUT*
5 - 2Ø	BG2IN*
6 - 19	BG2ØUT*
7 - 18	BG3IN*
8 - 17	BG3ØUT*
9 - 16	BRØ*
1Ø - 15	BR1*
11 - 14	BR2*
12 - 13	BR3*

NOTE: Only one of the BR*, BG*IN, BG*OUT signals should be enabled at the same time.

2.16 RESET OF THE CPU 68Ø1Ø BOARD

The switch on the front panel is used to RESET all on-board devices except the CIO and SCC, and all devices on the VME bus.

The CIO and SCC are excluded because the CIO must constantly generate the PERCLK signal to the DRAM Controller which constantly generates refresh requests, and the contents of DRAM is not changed during the manual RESET.

After power-up, the internal RESET- signal is used to reset all the devices on the CPU 68Ø1Ø board and to force the SYSRESET* signal on the VME bus. This allows a general RESET of all peripheral boards and devices of the system. The power-up RESET is handled by IC 4ØØ6B on position E46 and is driven by the E (Enable) signal from the 68Ø1Ø processor. The duration of the power-up reset is approximately 4ØØ ms. The REZ2 signal from the IC 4ØØ6B on position E46 drives the RESET- signal through the IC 74LS641-1 on position E15.

CHAPTER 3

3. PROGRAMMING MODEL

3.0 MEMORY MAP OF THE CPU 68010

The address map of the CPU 68010 is the following:

000 000 : 000 007	Initialization Vectors from System ROM/EPROM
000 008 : 0FF FFF	System DRAM
100 000 : FDF FFF	Not Used
FE0 000 : FE0 007	Initialization Vectors in System ROM/EPROM
FE0 008 : FE0 00F	Z8530 SCC
FE0 010 : FE0 017	Z8536 CIO
FE0 018 : FE0 02F	Not Used

```
FEØ Ø3Ø
   :      NS32Ø81 FPU
FEØ Ø37
FEØ Ø38
   :      Not Used
FEØ Ø3F
FEØ Ø4Ø
:         MC68451 MMU
FEØ Ø7F
FEØ Ø8Ø
   :      Not Used
FEØ 1FF
FEØ 2ØØ
   :      MC46818 RTC
FEØ 3FF
FEØ 4ØØ
   :      System EPROM
FEF FFF
FFØ ØØØ
   :      I/O Area    /CPU 68Ø1Ø MASTER/
FFF FFF
```


Izdaja	1				
Št. obvestila	11-002.				

IskraDelta
proizvodnja računalniških sistemov in inženiring, p.o.

List	Stran	J	K	Identifikacijska številka
30				32804044

Arhiv

Namesto identifikacijske številke: 18842044

sero 82-3407-12-85-0

3.1 DRAM ADDRESSING

The DRAM addressing can be performed on byte and word basis. Read, write and read-modify-write cycles are provided.

After power-up of the CPU 68010 board, the DRAM address area should be overwritten for the reason of parity logic.

The addressing of the DRAM depends on the used DRAM ICs:

Start Address $000008

End Address a) $0FFFFF (1M byte) - 256K*1 ICs

b) $03FFFF (256K bytes) - 64K*1 ICs

If the elements 64K*1 are used and the decoding logic is not changed, the contents of the DRAM are repeated in the $040000 adress steps. The addresses of the DRAM are the same when addressed from the 68010 or from the VME bus, but can be changed in the decoding logic.

3.2 ROM/EPROM ADDRESSING

The ROM/EPROM addressing can be performed on byte and word basis, only read cycles are provided. The initial stack pointer and reset vector, which are read by the processor 68010 after reset on addresses $000000-$000007, are stored in the ROM/EPROM on addresses $FE0000-$FE0007. Part of the ROM/EPROM address area ($FE0008-$FE03FF) is used for the address areas of the CIO, SCC, FPU, MMU and RTC.

The addressing of the ROM/EPROM depends on the used ROM/EPROM ICs:

```
Start address      a)   $000000
End address        a)   $000008

Start address      b1)  $FE0400
End address        b1)  $FE3FFF     ;   2764  ICs

Start address      b2)  $FE0400
End address        b2)  $FE7FFF     ;   27128 ICs

Start address      b3)  $FE0400
End address        b3)  $FEFFFF     ;   27256 ICs

Start address      b4)  $FD0400
End address        b4)  $FEFFFF     ;   27512 ICs
```

The decoding logic is provided for 27256 ICs and the contents of the ROM/EPROM is repeated when ICs with smaller capacities are used. When using ICs 27512, the decoding logic of the CPU 68010 board should be changed.

3.3 ADDRESSING THE 68451 MMU

The 68451 MMU address area ranges from $FE0040 - $FE007F.

Word and byte addressing is possible.

Descripton of individual addresses:

Address	Mode	Description
FE0042	R/W	AST1 (User Data)
FE0044	R/W	AST2 (User Program)
FE004A	R/W	AST5 (Supervisory Data)
FE004C	R/W	AST6 (Supervisory Program)
FE004E	R/W	AST7 (Interrupt Acknowledge)
FE0060	R/W	AC0 LBA - MSB (Logical Base Address)
FE0061	R/W	AC1 LBA - LSB (Logical Base Address)
FE0062	R/W	AC2 LAM - MSB (Logical Address Mask)
FE0063	R/W	AC3 LAM - LSB (Logical Address Mask)
FE0064	R/W	AC4 PBA - MSB (Physical Base Address)
FE0065	R/W	AC5 PBA - LSB (Physical Base Address)
FE0066	R/W	AC6 Address Space Number Register
FE0067	R/W	AC7 Status Register
FE0068	R/W	AC8 Address Space Mask Register
FE0069	R/W	DP Descriptor Pointer
FE006B	R/W	IVR Interrupt Vector Register

FE00D6D	R/W	GSR Global Status Register
FE00D6F	R/W	LSR Local Status Register
FE00D71	R/W	SSR Segment Status and Transfer Descriptor Operation
FE00D79	R/W	IDP Interrupt Descriptor Pointer
FE00D7B	R/W	RDP Result Descriptor Pointer
FE00D7D	R/W	DTO Direct Translation Operation
FE00D7F	R/W	LDO Load Descriptor Operation

3.4 ADDRESSING THE MC146818 RTC

The RTC address area occupies addresses $FE0200 - $FE03FF. Addressing is possible on byte basis, i.e. on odd addrersses. When addressing is carried out on word basis, only the lower data byte is transferred (D00-D07).

Description of individual addresses:

Address	Mode	Description
FE0201	R/W	Seconds
FE0203	R/W	Second Alarm
FE0205	R/W	Minutes
FE0207	R/W	Minute Alarm
FE0209	R/W	Hours
FE020B	R/W	Hour Alarm
FE020D	R/W	Day in Week
FE020F	R/W	Day in Month
FE0211	R/W	Month
FE0213	R/W	Year

Address	Mode	Description
FE0215	R/W	Register A
FE0217	R/W	Register B
FE0219	R	Register C
FE021B	R	Register D
FE201D-RE20FF	R/W	Generally Usable CMOS RAM with the Possibility of a Battery Back-up

3.5 ADDRESSING THE Z8536 CIO

The Z8536 CIO address area occupies the $FE0010 - $FE0017 addresses. Addressing on byte basis is possibble, with addressing on word basis only the lower data byte is transferred (D00-D07).

Addresses and description of individual CIO registers are:

Address	Mode	Description
FE0011	R/W	Port C Data Register
FE0013	R/W	Port B Data Register
FE0015	R/W	Port A Data Register
FE0017	R/W	Control Register

3.6 ADDRESSING THE Z8530 SCC

The Z8530 SCC address area occupies the $FE0008 - $FE000F addresses. Byte addressing is possible, word addressing transfers only the lower data byte (D00-D07).

Addresses and description of individual SCC registers are:

Port A:

Address	Mode	Description
FE0000D	R	Read Register Status
FE0000D	W	Write Register Commands
FE0000F	R	Read Register Data
FE0000F	W	Write Register Data

Port B:

Address	Mode	Description
FE00009	R	Read Register Status
FE00009	W	Write Register Commands
FE0000B	R	Read Register Data
FE0000B	W	Write Register Data

3.7 NS32081 FPU ADDRESS AREA

The NS32081 FPU address area occupies the $FE0030 - $FE0037 addresses. Only word addressing is possible.

Addresses and descriptions of individual FPU registers are:

Address	Mode	Description
FE0030	R/W	Not Used
FE0032	R	Read Result
FE0032	W	Write Operation Word
FE0034	R	Read Status Word
FE0036	W	ID byte

APPENDIX A

P A L s

Ident.	Device	Description
32537Ø44	IC PAL16R4A	ARBI 68Ø1Ø
32538Ø44	IC PAL14L4A	DEK1 68Ø1Ø
32539Ø44	IC PAL16L8A	DEK2 68Ø1Ø
32540Ø44	IC PAL16R4A	PARI 68Ø1Ø
32541Ø44	IC PAL16L8A	PINT 68Ø1Ø
32542Ø44	IC PAL16R6A	REF 68Ø1Ø
32543Ø44	IC PAL16L8A	VFUN 68Ø1Ø
32544Ø44	IC PAL16R6A	ZILO 68Ø1Ø

IDENTIFICATION: 32537044

DEVICE TYPE: PAL 16R4A

DESCRIPTION: ARBI 68010

FILE NAME: ARBI

LOCATION ON THE CPU 68010 BOARD: E14

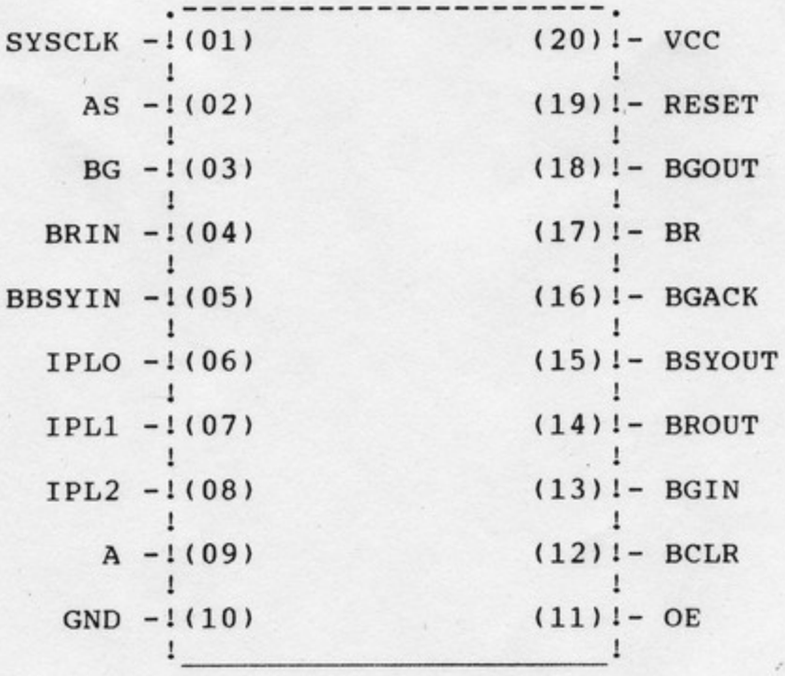
FUNCTION: ARBITRATION LOGIC

DATE: 19.02.1987

PIN NAMES:

SYSCLK , AS , BG , BRIN ,BBSYIN , IPLO , IPL1 , IPL2 , A , GND ,
OE , BCLR , BGIN , BROUT , BSYOUT , BGACK , BR , BGOUT ,
RESET, VCC

LOGIC PINOUT:



Izdaja	3					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-033					37				32804044
Iskra Delta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv				Namesto identifikacijske številke: 18842044

```
EQUATIONS:
==========


/BRØUT :=  BSYOUT * BBSYIN * BGIN * BCLR * /A * RESET
         +  BSYOUT * /IPL2 * BGIN * /BGACK * BCLR * /A * RESET
         + /BROUT * BGOUT * /A * RESET;

/BSYOUT := /BROUT * /BGIN * /A * RESET
          + /BSYOUT * BGOUT * /A * RESET
          +  BGACK * BGOUT * BGIN * A * RESET;

IF (VCC) /BGOUT = /BG * AS * BGACK * /BR * /BRIN * RESET
                  *  BBSYIN * BSYOUT
                  + /BG * AS * BGACK * /BR * /BCLR * RESET
                  +  BGOUT * /BG * AS  *  BBSYIN * BSYOUT * /BR
                  * /BRIN * /BGACK * A * RESET
                  + /BGOUT * /BRIN * /BR * AS * BBSYIN * BSYOUT
                  *  RESET
                  + /BGOUT * /BCLR * /BR * AS * BBSYIN * BSYOUT
                  *  RESET
                  + /BGIN * BROUT * /A * RESET;

/BR := /BRIN * BROUT * BGACK * /BSYOUT * RESET
     + /BCLR * RESET
     + /BBSYIN * /BGACK * BSYOUT * RESET
     + /BR * BROUT * /BRIN * RESET;

/BGACK  :=  BGACK * BSYOUT * BBSYIN * /BRIN * /BR * /BG *  /BGOUT
         *  AS * RESET
         +  BGACK * /BCLR * /BG * /BGOUT * AS * RESET
         + /BGACK * /BCLR * RESET
         + /BGACK * /BR * BSYOUT * RESET
         + /BGACK * BR * /BBSYIN * BSYOUT * RESET
         + /RESET * /A;

IF (A * AS)
      /BGIN = /BG * AS * BGACK * /BR * /BRIN * RESET
            + /BG * AS * BGACK * /BR * /BCLR * RESET
            +  BGIN * /BG * AS * BBSYIN * BSYOUT * /BR * /BRIN
            * /BGACK * RESET
            + /BGIN * /BRIN * /BR * AS * BBSYIN * BSYOUT * RESET
            + /BGIN * /BCLR * /BR * AS * BBSYIN * BSYOUT * RESET.
```

IDENTIFICATION: 32538044

DEVICE TYPE: PAL 14L4A

DESCRIPTION: DEK1 68Ø1Ø

FILE NAME: DEK1

LOCATION ON THE CPU 68Ø1Ø BOARD: E35

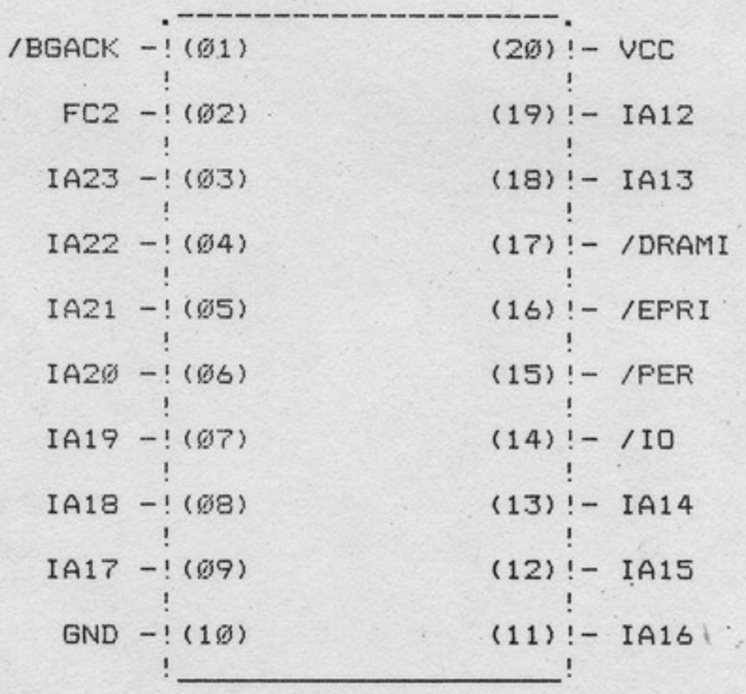
FUNCTION: DECODER OF UPPER ADDRESSES

DATE: Ø6.Ø2.1986

PIN NAMES:

/BGACK , FC2 , IA23 , IA22 , IA21 , IA2Ø , IA19 , IA18 , IA17 , GND , IA16 , IA15 , IA14 , /IO, /PER , /EPRI , /DRAMI , IA13 , IA12 , VCC.

LOGIC PINOUT:



EQUATIONS:
==========

```
IO     = BGACK * IA23 * IA22 * IA21 * IA20 * IA19 * IA18 * IA17
       * IA16 ;

PER    = IA23 * IA22 * IA21 * IA20 * IA19 * IA18 * IA17
       * /IA16 * /IA15 * /IA14 * /IA13 * /IA12 ;

EPRI   = /IA23 * /IA22 * /IA21 * /IA20 * /IA19 * /IA18 * /IA17
       * /IA16 * /IA15 * /IA14 * /IA13 * /IA12
       + IA23 * IA22 * IA21 * IA20 * IA19 * IA18 * IA17 * /IA16 ;

DRAMI  = /IA23 * /IA22 * /IA21 * /IA20.
```

IDENTIFICATION: 32539044

DEVICE TYPE: PAL 16L8A

DESCRIPTION: DEK2 68Ø1Ø

FILE NAME: DEK2

LOCATION ON THE CPU 68Ø1Ø BOARD: E32

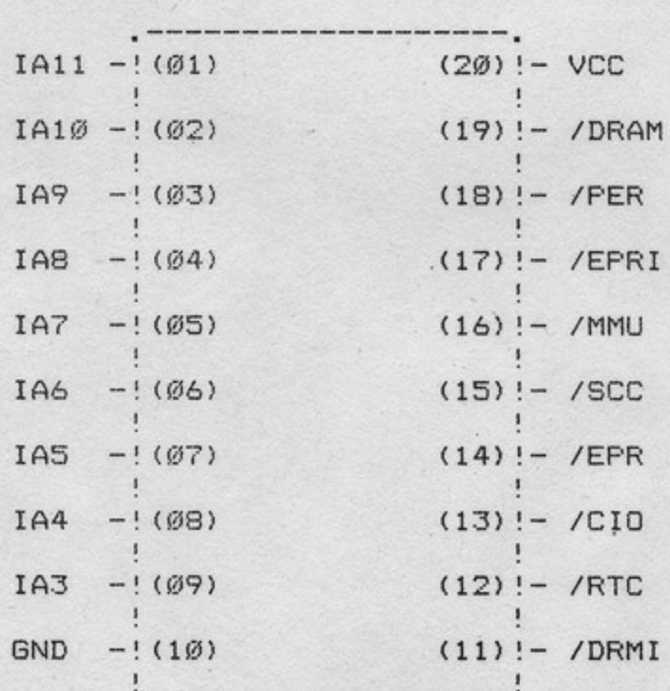
FUNCTION: DECODER OF LOWER ADDRESSES

DATE: Ø6.Ø2.1986

PIN NAMES:

IA11 , IA1Ø , IA9 , IA8 , IA7 , IA6 , IA5 , IA4 , IA3 , GND ,
/DRMI , /RTC , /CIO , /EPR , /SCC , /MMU , /EPRI , /PER , /DRAM ,
VCC.

LOGIC PINOUT:



Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-002					41				32804044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv				Namesto identifikacijske številke: 18842044

sero 82-3407-12-86-0

```
EQUATIONS:
==========

IF(VCC) RTC  = PER * /IA11 * /IA10 * IA9 ;

IF(VCC) SCC  = PER * /IA11 * /IA10 * /IA9 * /IA8 * /IA7 * /IA6
             * /IA5 * /IA4 * IA3 ;

IF(VCC) CIO  = PER * /IA11 * /IA10 * /IA9 * /IA8 * /IA7 * /IA6
             * IA4 * /IA3 ;

IF(VCC) MMU  = PER * /IA11 * /IA10 * /IA9 * /IA8 * /IA7 * IA6 ;

IF(VCC) EPR  = EPRI * DRMI * /IA11 * /IA10 * /IA9 * /IA8 * /IA7
             * /IA6 * /IA5 * /IA4 * /IA3
             + EPRI * /DRMI * /PER
             + EPRI * /DRMI * PER * IA11
             + EPRI * /DRMI * PER * IA10 ;

IF(VCC) DRAM = DRMI * /EPRI
             + DRMI * EPRI * /EPR.
```

IDENTIFICATION: 32540044

DEVICE TYPE: PAL 16R4A

DESCRIPTION: PARI 68010

FILE NAME: PARI

LOCATION ON THE CPU 68010 BOARD: E38

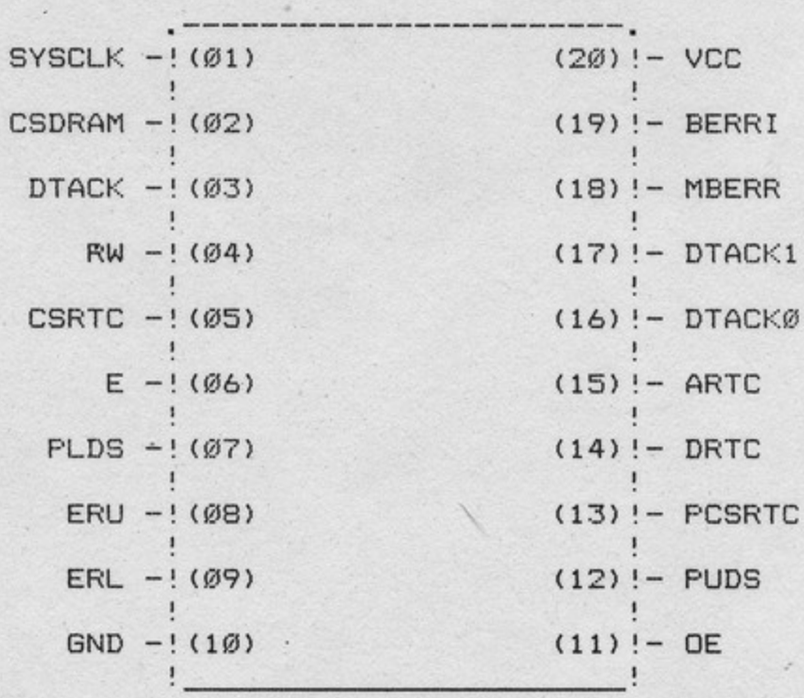
FUNCTION: CONTROL OF DRAM PARITY, RTC

DATE: 06.02.1986

PIN NAMES:

SYSCLK , CSDRAM , DTACK , RW, CSRTC , E , PLDS , ERU , ERL, GND,
OE , PUDS , PCSRTC , DRTC , ARTC , DTACK0 , DTACK1 , MBERR ,
BERRI , VCC.

LOGIC PINOUT:



```
EQUATIONS:
==========


/DTACKO := MBERR * /DTACK1 * /PLDS
         + MBERR * /DTACK1 * /PUDS
         + /DTACKO * /PLDS
         + /DATCKO * /PUDS ;

/DTACK1 := /DTACK * /PLDS
         + /DTACK * /PUDS ;

/ARTC := /PLDS * /CSRTC * /E ;

/DRTC := /PLDS * /CSRTC *  E ;

IF (VCC) /PCSRTC = /PLDS * /CSRTC ;

IF (VCC) /MBERR = /CSDRAM * /DTACK1 * RW * ERL * /PLDS
                + /CSDRAM * /DTACK1 * RW * ERU * /PUDS
                + /BERRI  * /PUDS * CSDRAM
                + /BERRI  * /PLDS * CSDRAM.
```

IDENTIFICATION: 32541Ø44

DEVICE TYPE: PAL 16L8A

DESCRIPTION: PINT 68Ø1Ø

FILE NAME: PINT

POSITION ON THE CPU 68Ø1Ø BOARD: E44

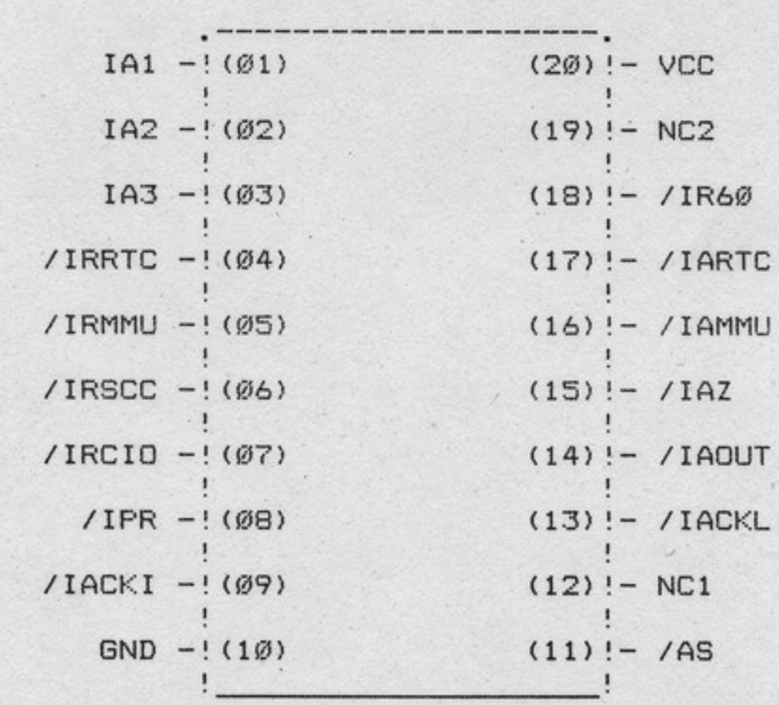
FUNCTION: INTERRUPT LOGIC

DATE: Ø6.Ø2.1986

PIN NAMES:

IA1 , IA2 , IA3 , /IRRTC , /IRMMU , /IRSCC , /IRCIO , /IPR , /IACKI , GND , /AS , NC1 , /IACKL , /IAOUT , /IAZ , /IAMMU , /IARTC , /IR6Ø , NC2 , VCC.

LOGIC PINOUT:



Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-002					45				32804044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv				Namesto identifikacijske številke: 18842044

EQUATIONS:
==========

```
IF(AS)  IARTC = IA3 * IA2 * /IA1 * IACKI * IRRTC * /IAMMU * /IAZ
                * /IAOUT

                + IARTC * IACKI ;

IF(AS)  IAMMU = IA3 * IA2 * /IA1 * IACKI * IRMMU * /IRCIO * /IRSCC
                * /IRRTC * /IARTC * /IAZ * /IAOUT

                + IAMMU * IACKI * /IAZ * /IARTC ;

IF(AS)  IAZ   = IA3 * IA2 * /IA1 * IACKI * IRCIO * /IRRTC
                * /IARTC * /IAMMU * /IAOUT

                + IA3 * IA2 * /IA1 * IACKI * IRSCC * /IRRTC
                * /IARTC * /IAMMU * /IAOUT

                + IAZ * IACKI * /IARTC ;

IF(AS)  IAOUT = IACKI * IA3 * IA2 * IA1

                + IA3 * IA2 * /IA1 * IACKI * IPR * /IRRTC * /IRMMU
                * /IRCIO * /IRSCC * /IARTC * /IAMMU * /IAZ

                + IACKI * IA3 * /IA2
                + IACKI * /IA3
                + IAOUT * IACKI * /IAZ * /IAMMU * /IARTC ;

IF(VCC)  IR6Ø = IRRTC + IRMMU + IRSCC + IRCIO + IPR ;

IF(AS)  IACKL = AS * IACKI.
```

IDENTIFICATION: 32542Ø44

DEVICE TYPE: PAL 16R6A

DESCRIPTION: REF 68Ø1Ø

FILE NAME: REF

LOCATION ON THE CPU 68Ø1Ø BOARD: E4

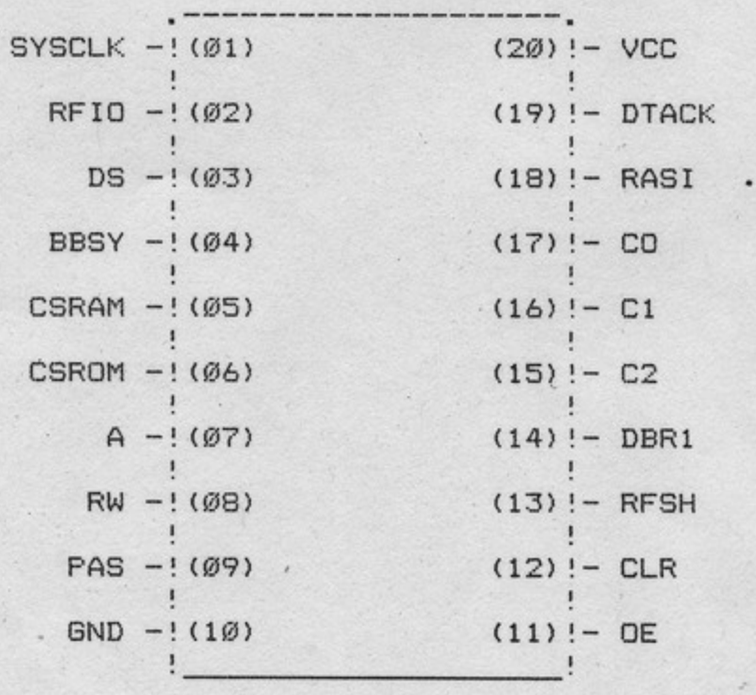
FUNCTION: DRAM REFRESH LOGIC

DATE: Ø6.Ø2.1986

PIN NAMES:

SYSCLK , RFIO , DS , BBSY , CSRAM , CSROM , A , RW , PAS , GND ,
OE , CLR , RFSH , DBR1 , C2 , C1 , CØ , RASI , DTACK , VCC.

LOGIC PINOUT:



```
EQUATIONS:
==========

/CO := CO*CLR ;

/C1 :=  CØ* C1*CLR
     + /CO*/C1*CLR ;

/C2 :=  CO*C1*C2*CLR
     + /C1*/C2*CLR
     + /CO*C1*/C2*CLR ;

/DBR1 := /RFIO*RASI*DS*/PAS
       + /RFIO*RASI*/DS*PAS*CSRAM
       + /DBR1*RFSH ;

/RASI := /DBR1*/CLR*RASI*/DS*PAS*/RFIO
       + /DBR1*CLR*RASI*/RFIO*CSRAM*DS*/PAS
       + /RASI*CO*C1*C2*/RFIO
       + /RASI*CO*C1*C2*/RFSH
       + /RASI*/C2
       +  RASI*CSRAM*CSROM*DS*/CO*C1*C2*RFIO*RFSH*CLR*/PAS
       + /RASI*CSRAM*CSROM*DS*RFIO*RFSH*/PAS ;

IF(VCC) /CLR =  RASI*/DS
              + /RASI*/CO*/C1*C2
              + /RASI*/RFIO*/RFSH ;

/RFSH := /RASI*/CO*/C1*/C2*/RFIO
       + /RASI*/RFSH*/RFIO
       + /RASI*CO*C1*C2*RFIO*/RFSH
       + /RASI*/C1*/C2*RFIO*/RFSH ;

IF(VCC) /DTACK = /CSRAM*DS*RASI*/CO*/C1*/C2*/RW*/PAS
                + /CSRAM*DS*RASI*/CO*/C1*/C2*/A*BBSY*RW*/PAS
                + /CSRAM*DS*RASI*/CO*C1*/C2*A*BBSY*RW*/PAS
                + /CSRAM*DS*RASI*/CO*C1*/C2*/A*/BBSY*RW*/PAS
                + /CSRAM*DS*RASI*/CO*/C1*C2*A*/BBSY*RW*/PAS
                + /CSROM*DS*/CO*/C1*C2*RW*RASI*CLR*/PAS
                + /DTACK*DS*/PAS.
```

IDENTIFICATION: 32543Ø44

DEVICE TYPE: PAL 16L8A

DESCRIPTION: VFUN 68Ø1Ø

FILE NAME: VFUN

LOCATION ON THE CPU 68Ø1Ø BOARD: E36

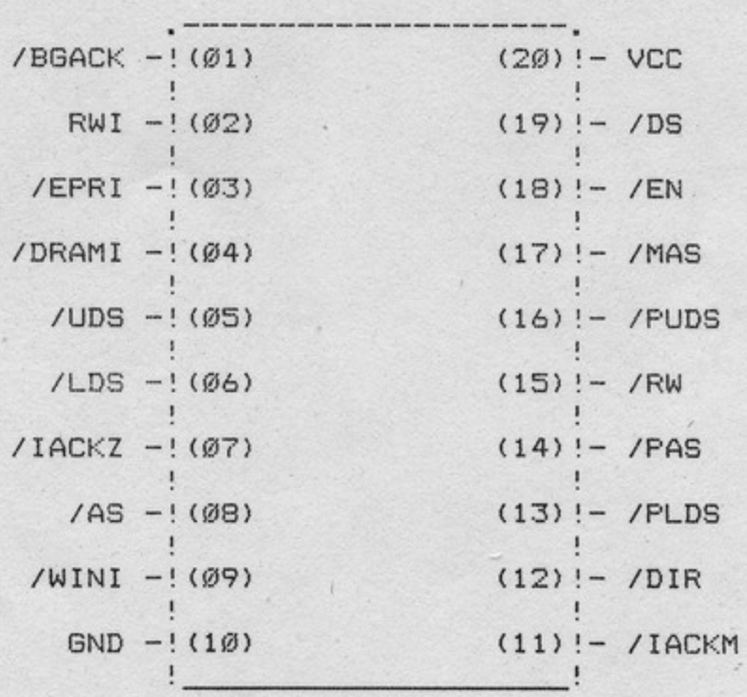
FUNCTION: VARIOUS CONTROL SIGNALS

DATE: Ø6.Ø2.1986

PIN NAMES:

/BGACK , RWI , /EPRI , /DRAMI , /UDS , /LDS , /IACKZ , /AS , /WINI , GND , /IACKM , /DIR , /PLDS , /PAS , /RW , /PUDS , /MAS , /EN, /DS, VCC.

LOGIC PINOUT:



Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-002					49				32804044
						Arhiv				Namesto identifikacijske številke
										18842044

```
EQUATIONS:
==========

IF(VCC)         EN   = /BGACK * /EPRI * /DRAMI * /IACKZ * /IACKM
                     +  BGACK *  EPRI
                     +  BGACK *  DRAMI ;

IF(VCC)         DIR    =  RWI * /BGACK
                       + /RWI *  BGACK ;

IF(/BGACK)      PLDS   = AS * LDS * RWI * MAS
                       + AS * LDS * /RWI * /WINI * MAS ;

IF(/BGACK)      PUDS   = AS * UDS * RWI * MAS
                       + AS * UDS * /RWI * /WINI * MAS ;

IF(/BGACK)      PAS    = AS * MAS ;

IF(VCC)         RW   = PAS * /RWI ;

IF(VCC)         DS   = /PLDS * /PUDS.
```


Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-002					50				32804044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv				Namesto identifikacijske številke: 18842044

IDENTIFICATION: 32544044

DEVICE TYPE: PAL 16R6A

DESCRIPTION: ZILO 68010

FILE NAME: ZILO

LOCATION ON THE CPU 68010 BOARD: E39

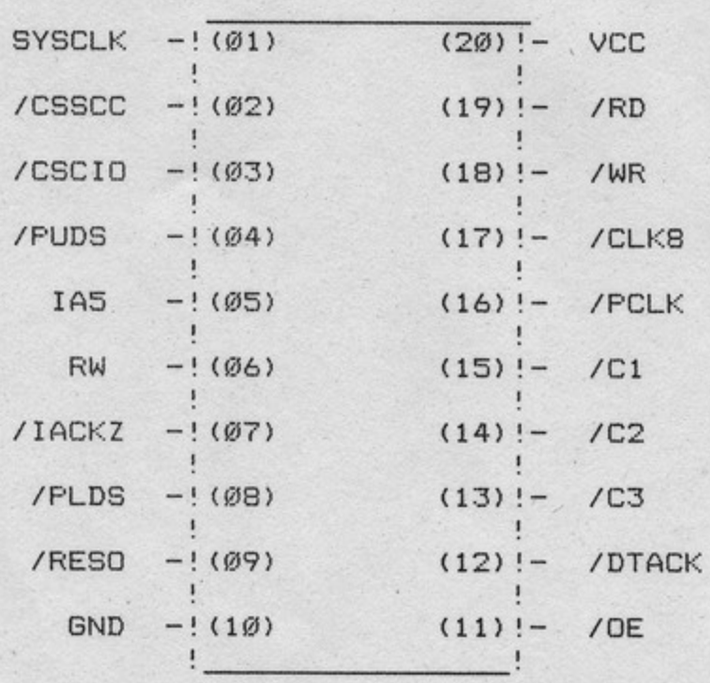
FUNCTION: CONTROL LOGIC OF Z8530, Z8536

DATE: 06.02.1986

PIN NAMES:

SYSCLK , /CSSCC , /CSCIO , /PUDS , IA5 , RW , /IACKZ , /PLDS,
/RESO , GND , /OE , /DTACK , /C3 , /C2 , /C1 , /PCLK , /CLK8,
/WR , /RD , VCC.

LOGIC PINOUT:



```
EQUATIONS:
==========

CLK8 := /CLK8 ;

PCLK := /PCLK *  CLK8
      +  PCLK * /CLK8 ;

C1 := /RESO * PLDS * /C1 *  PCLK * CLK8
    + /RESO * PLDS *  C1 * /PCLK
    + /RESO * PLDS *  C1 * /CLK8
    + /RESO * IACKZ * /C1 * PCLK * CLK8
    + /RESO * CSCIO * /C1 * PCLK * CLK8 * /IA5
    + /RESO * CSSCC * /C1 * PCLK * CLK8 ;

C2 := /RESO * PLDS * /C2 *  C1 * PCLK * CLK8
    + /RESO * PLDS *  C2 * /C1
    + /RESO * PLDS *  C2 * /PCLK
    + /RESO * PLDS *  C2 * /CLK8 ;

C3 := /RESO * PLDS * /C3 *  C2 * C1 * PCLK * CLK8
    + /RESO * PLDS *  C3 * /C2
    + /RESO * PLDS *  C3 * /C1
    + /RESO * PLDS *  C3 * /PCLK
    + /RESO * PLDS *  C3 * /CLK8 ;

WR := /RESO*PLDS*/RW*/IACKZ*/C3*/C2*C1*/PCLK*/CLK8*CSSCC
    + /RESO*PLDS*/RW*/IACKZ*/C3*/C2*C1*/PCLK*/CLK8*/IA5*CSCIO
    + /RESO*PLDS*/RW*/IACKZ*WR*/C3*/C2*C1
    + /RESO*PLDS*/RW*/IACKZ*WR*/C3*C2*/C1
    +  RESO ;

IF (VCC) RD = /RESO*PLDS*RW*/IACKZ*/C3*/C2*C1*/PCLK*CLK8*CSSCC
       + /RESO*PLDS*RW*/IACKZ*/C3*/C2*C1*/PCLK*CLK8*/IA5*CSCIO
       + /RESO*PLDS*RW*IACKZ*/C3*C2*/C1*PCLK*CLK8
       + /RESO*PLDS*RW*RD
       +  RESO ;

IF (VCC) DTACK = /RESO*PLDS*/IACKZ*/C3*C2*/C1*PCLK*/CLK8*CSSCC
       + /RESO*PLDS*/IACKZ*/C3*C2*/C1*PCLK*/CLK8*/IA5*CSCIO
       + /RESO*PLDS*IACKZ*RW*/C3*C2*C1*PCLK*/CLK8
       + /RESO*PLDS*PUDS*IA5*CSCIO
       + /RESO*PLDS*DTACK.
```